1. A circuit for quantifying a high-voltage signal comprising:

a first terminal having a first voltage;

an output terminal;

a field transistor having a drain, a gate, and a source, said gate connected to said first terminal, said drain and source having a second and third voltage, said output terminal coupled to said field transistor;

wherein said output terminal provides a signal representative of said first voltage.

2. The circuit as defined in claim 1 wherein said field transistor further comprises:

a polysilicon gate; and

a gate oxide;

wherein said gate oxide is formed during a LOCOS step including a masked region masked by silicon-nitride, said gate oxide formed in a region absent of silicon-nitride.

3. The circuit of claim 2 wherein said gate oxide has a thickness of at least 0.1 micron.

4. The circuit of claim 2 wherein said gate oxide has a thickness of at least 0.5 micron.

5. The circuit of claim 1 wherein said field transistor comprises a metal gate layer deposited over a thermal oxide.

6. The circuit of claim 1 wherein said field transistor comprises a metal gate transistor in which the metal gate is formed over an active region and a thick, oxide layer deposited as a pre-metal dielectric after poly deposition above the active region.

7. The circuit of claim 1 wherein said field transistor comprises a metal gate transistor in which the metal gate is formed over a deposited oxide which lies upon a LOCOS oxide.

8. The circuit as defined in claim 1 wherein said field transistor comprises a NMOS transistor

9. The circuit as defined in claim 1 wherein said field transistor comprises a PMOS transistor

10. The circuit as defined in claim 1 wherein said field transistor is formed over a n-type region.

11. The circuit as defined in claim 1 wherein said field transistor is formed over a p-type region.

12. The circuit as defined in claim 2 wherein said field transistor further includes a drain extension region formed under said gate oxide by a dopant species introduced before said LOCOS step.

13. The circuit as defined in claim 6 wherein said field transistor further includes a drain extension region formed under said active region by a dopant species implanted into said active region.

14. A circuit, comprising:
at least one low voltage input;
a first high voltage terminal; and
a first field transistor having a source, a drain and a control region;
wherein said control region is coupled to said first high voltage terminal.

15. The circuit of claim 14 wherein said circuit further includes a second field transistor coupled to said first field transistor.

16. The circuit of claim 15 wherein each field transistor includes a cascode transistor coupled thereto.

17. The circuit of claim 14 wherein said first field transistor comprises a NMOS transistor.

18. The circuit of claim 14 wherein said first field transistor comprises a PMOS transistor.

19. The circuit of claim 15 wherein each field transistor has a width, and wherein said second field transistor has a width which is greater than the width of the first field transistor.

20. The circuit of claim 19 wherein the width of the second field transistor is about 10 times greater than that of the first field transistor.

21. The circuit of claim 14 wherein said field transistor comprises a MOS transistor having an oxide separating said source and said drain regions and said control region, and said oxide has a thickness greater than the maximum thickness available to other MOS devices on an integrated circuit chip on which the circuit is manufactured.

22. The circuit of claim 21 wherein the field transistor is a NMOS transistor.

23. The circuit of claim 21 wherein the field transistor is a PMOS transistor.

24. The circuit of claim 21 wherein the oxide has a thickness of at least 1000 Angstroms.

25. The circuit of claim 14 further including a second field transistor, each field transistor having coupled thereto a cascode transistor and a mirror transistor, wherein each field transistor is coupled to a first rail and each mirror transistor is coupled to a second rail.

26. The circuit of claim 25 wherein each field transistor further comprises a width and a drain current, and the width of the second field transistor is greater than that of the first field transistor, such that a bias applied to the cascode transistors generates a gain between said drain currents dependent upon the ratio of the width of the second transistor to the first transistor.

27. The circuit of claim 25 wherein said first high voltage terminal has a swing of at least 40v.

28. The circuit of claim 25 wherein an input voltage has a swing of no greater than 15 v.

29. The circuit of claim 14 further including a second field transistor, each field transistor having coupled thereto a cascode transistor and a mirror transistor, wherein each field transistor is coupled to a first rail and each mirror transistor is coupled to a second rail and the gate of each cascode transistor is coupled to a cascode voltage.

30. The circuit of claim 29 wherein the mirror transistor coupled to the first field transistor is a diode connected input to a current mirror.

31. The circuit of claim 30 wherein the second field transistor is connected to a mirror output.

60. The circuit as defined in claim 1 wherein said signal representative of said first voltage is a voltage signal.

61. The circuit as defined in claim 1 wherein said signal representative of said first voltage is a current.

62. The circuit of claim 1 further including a low-voltage input, wherein said first terminal includes an amplified representation of said low-voltage input.

63. The circuit of claim 15 further including a current-differencing circuit coupled to said first field transistor and said second field transistor, said current-differencing circuit having an output.

64. The circuit of claim 63 further including a trans-impedance stage having an input and an output, said trans-impedance stage input coupled to said current-differencing circuit output.

65. The circuit of claim 63 said current-differencing circuit further including:

a first input current;

a second input current;

wherein said output of said current-differencing circuit includes an amplified signal representative of the difference between said first input current and said second input current.

66. The circuit of claim 14 wherein said first high voltage terminal includes an amplified representation of said low voltage input.

67. The circuit of claim 14, further including:

a second high voltage terminal; and

a differential mode feedback circuit.

68. The circuit of claim 67 wherein the voltage between said first high voltage terminal and said second high voltage terminal includes an amplified representation of said low voltage input.

69 The circuit of claim 67 further including a common mode feedback circuit.

70. The circuit of claim 14 further including

a reference circuit;

a current-steering circuit having an input and an output.

71. The circuit of claim 68 wherein said current-steering circuit further includes a coupling from said low-voltage input to said input, and said current steering circuit is coupled to said reference circuit.

72. The circuit of claim 69 wherein said reference circuit further includes a second field transistor having a gate and a reference voltage connected to said second field transistor gate.

73. The circuit of claim 68 further including a differencing circuit having a first input, a second input, and an output, said first input coupled to said first field transistor and said second output coupled to the output of said current-steering circuit.

74. The circuit of claim 14, further comprising at least one MEMS mirror coupled to said high-voltage terminal.

---

75. The circuit of claim 1 further including:

a reference circuit;

a current-steering circuit having an input and an output coupled to said reference circuit.

B1

76. The circuit of claim 75 wherein the reference circuit includes at least a second field transistor.
